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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,269	05/25/2001	Sasan Cyrusian	10808/27	5524

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EXAMINER
COX, CASSANDRA F

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/866,269	CYRUSIAN, SASAN	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *20-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-19, drawn to differential controlled delay unit, classified in class 327, subclass 274.

II. Claims 20-23, drawn to phase locked loop, classified in class 327, subclass 157.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the phase locked loop does not require the particulars of the differential controlled delay unit. The subcombination has separate utility such as in a timing generator.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with David Okey on June 5, 2002 a provisional election was made with traverse to prosecute the invention of group I,

claims 1-19. Affirmation of this election must be made by applicant in replying to this Office action. Claims 20-23 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 15-17 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 15 is not enabled because there is no support in the specification for connecting the drains of the first amplifier to the sources of the second amplifier.

Claims 16-17 are also rejected due to the deficiencies of the base claim and any intervening claims.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-3 and 10-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is indefinite because the statement "a control input and power supply voltage is connected to drains of the first amplifier" is misdescriptive. It appears to the examiner from review of the drawings and specification that the

control input is connected to the sources of the first amplifier rather than to the drains as stated in the claim.

Claims 2-3 are also rejected due to the deficiencies of the base claim and any intervening claims.

Claim 10 is indefinite because the phrase "connected to gates of the additional delay unit" is unclear. Since there are multiple transistors in each delay unit, it is not clear to the examiner which gates the applicant is referring to. The same applies to the phrase "connected to gates of the first delay unit". The same applies to claim 11 (including reference to the phrase "connected to gates of the second delay unit"). The same also applies to claims 12-16. Correction or clarification is required.

Claim 17 is also rejected due to the limitations of the base claim and any intervening claims.

9. Claim 16 recites the limitation "the first input unit" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the

United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

11. Claims 1 and 4-6 are rejected under 35 U.S.C. 102(e) as being anticipated by An et al. (U.S. Patent No. 6,100,769).

In reference to claim 1, An discloses in Figure 7 a circuit comprising: a first amplifier having a first (MN6) and second (MN7) transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor (MN6) is connected to a drain of the second transistor (MN7) and a gate of the second transistor (MN7) is connected to a drain of the first transistor (MN6); and a second amplifier having a third (MP10) and fourth (MP11) transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals (V_{AON}, V_{AOP}), wherein a differential input voltage (V_{AIN}, V_{AIP}) is connected to gates of the second amplifier transistors, and a control input and power supply voltage (VSS) is connected to sources (based on the examiner's understanding of the figures and specification) of the first amplifier. The same applies to claim 4, wherein a control input and supply voltage (VDD) is connected to the sources of the second amplifier (through transistor MP8).

In reference to claim 5, the first amplifier transistors (MN6, MN7) are NMOS transistors and the second amplifier transistors (MP10, MP11) are PMOS transistors.

In reference to claim 6, a positive supply voltage (VDD) is connected to the second amplifier (through transistor MP8) and a negative supply voltage is connected to the first amplifier (MN6, MN7).

12. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Soumyanath et al. (U.S. Patent No. 6,218,892).

In reference to claim 1, Soumyanath discloses in Figure 14 a circuit comprising: a first amplifier having a first (M11) and second (M12) transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor (M11) is connected to a drain of the second transistor (M12) and a gate of the second transistor (M12) is connected to a drain of the first transistor (M11); and a second amplifier having a third (M14) and fourth (M15) transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals (Vout+, Vout-), wherein a differential input voltage (Vin+, Vin-) is connected to gates of the second amplifier transistors, and a control input and power supply voltage (Vcc) is connected to sources (based on the examiner's understanding of the figures and specification) of the first amplifier. The same applies to claim 4, wherein a control input and supply voltage (Vss) is connected to the sources of the second amplifier.

In reference to claim 2, the first amplifier transistors (M11, M12) are PMOS transistors and the second amplifier transistors (M14, M15) are NMOS transistors.

In reference to claim 3, a positive supply voltage (Vcc) is connected to the first amplifier (M11, M12) and a negative supply voltage (Vss) is connected to the second amplifier (M14, M15).

13. Claims 1-4 and 7-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Okuda et al. (U.S. Patent No. 6,377,511).

In reference to claim 1, Okuda discloses in Figure 8 a circuit comprising: a first amplifier having a first (Q5) and second (Q6) transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor (Q5) is connected to a drain of the second transistor (Q6) and a gate of the second transistor (Q6) is connected to a drain of the first transistor (Q5); and a second amplifier having a third (Q1) and fourth (Q2) transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals (OUTN, OUTP), wherein a differential input voltage (INN, INP) is connected to gates of the second amplifier transistors, and a control input and power supply voltage (VDD; see column 13, line 64-column 14, line 7) is connected to sources (based on the examiner's understanding of the figures and specification) of the first amplifier. The same applies to claim 4, wherein a control input and supply voltage (GND) is connected to the sources of the second amplifier. The same also applies to claims 7 and 13 wherein the output terminals of the first delay unit (which is seen as the first differential controlled delay unit shown in Figure 8) are connected to gates of the second amplifier of the second delay unit (which is seen as the second differential controlled delay unit shown in

Figure 8) and output terminals (OUTN, OUTP) of the second delay unit are connected to gates (INN, INP) of the second amplifier of the first delay unit.

In reference to claim 2, the first amplifier transistors (Q5, Q6) are PMOS transistors and the second amplifier transistors (Q1, Q2) are NMOS transistors. The same applies to claims 8 and 11.

In reference to claim 3, a positive supply voltage (VDD) is connected to the first amplifier (Q5, Q6) and a negative supply voltage (GND) is connected to the second amplifier (Q1, Q2). The same applies to claim 9.

In reference to claim 10, Okuda shows in Figure 8 that the circuit can have additional delay units. The same applies to claims 12, 14, and 19.

Allowable Subject Matter

14. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter: Claim 18 would be allowable because the closest prior art of record fails to show a circuit as shown in Figure 9 wherein a buffered output voltage (the output of buffer 109) of the charge pump (98) is a supply voltage to the first amplifiers (82, 84) in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC
CC
June 16, 2002

Kenneth B. Wells
Primary Examiner